UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,851	12/20/2001	Claude Thibeault	17273-6US-AD	1516

20988 7590 11/23/2010

OGILVY RENAULT LLP
1, Place Ville Marie
SUITE 2500
MONTREAL, QC H3B 1R1
CANADA

EXAMINER	
GHULAMALI, QUTBUDDIN	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
11/23/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/022,851	THIBEAULT ET AL.	
	Examiner	Art Unit	
	Qutbuddin Ghulamali	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-20 and 25-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *12-20, 35-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application.
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to amendment filed 9/13/2010.

Response to Remarks/Amendment

2. Applicant's remarks/amendment filed 9/13/2010, has been considered but they are not persuasive. Applicant remarks, page 7-9, with reference to the newly introduced claim 35, the combination Balakrishnan, Tan and Hamamoto does not teach or suggested, a data transmitter comprising "a signal transmitter for sending each one of the plurality of first and second output signals on a respective one of substantially parallel conductors of a bus" and a "delay generator for delaying said second output signals by a delay period T_DLY relative to said first output signals", "wherein the clock period T_CLK is greater than the delay period T DLY". The examiner and examiner's supervisor reviewed the limitations, and respectfully disagree. First, claim 35, never recites "a data transmitter comprising a signal transmitter...". As to the limitation "sending each one of the plurality of first and second output signals on a respective one of substantially parallel conductors of a bus" attention is drawn to Balakrishnan, col. 3, lines 13-25; col. 4, lines 33-60, wherein Balakrishnan discloses a number of output signals (plurality of data and clock via parallel paths of a bus 16, fig, 2), and delay generator for delaying said second output signals by a delay period T_DLY relative to said first output signals (transmission path is compensated for by providing a controlled delay path (delay generator, a delay created as a result of the path delay, see abstract; the path delay is designed so as to generate a path delay that is longer than any data path delay in the device, col. 2, lines 23-26), wherein the clock period T_CLK is greater

than the delay period T DLY which allows a delay of x-secs (24 nsec in this case delay generated or built in) to ensure via control strobe to limit data rate to about 40 million transfers per second (col. 1, lines 60-68; col. 2, lines 9-39). As to applicant's remarks regarding the combination of prior arts, that the examiner responds that the strongest rationale for combining references is a recognition, expressly or implied in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been produced by their combination. In re Sernaker, 702 F. 2d 989, 994-95, 217 USPQ 1, 5-6 (Fed. Cir. 1983). In the instant case, the system of Balakrishnan, Tan and Hamamoto discloses the advantage for such combination. The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F. 2d 1071, 5 USPQ 2d 1596 (Fed. Cir. 1988) and In re Jones, 958 F. 2d 347, 21 USPQ 2d 1941 (Fed. Cir. 1992). In this case, the method of processing clock and data signal amounts to mitigating the skew or delay in the transmission path of the propagating signals via the parallel conductors or conductive paths as disclosed in the combined art could be utilized for achieving uniformity in signal output. Further, In view of the disclosure provided in the prior art to Balakrishnan as noted above, applicant's remarks are deemed not persuasive, and the rejection follows.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 35-36, 12-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 35, line 6, recites a signal transmitter …, with transmissions on each one of the substantially parallel conductor separated by a time period substantially equal to a clocl T_CLK; …The parallel conductors are driven by the same clock with a period, the transmission on each one of the substantially parallel conductor therefore, cannot possibly have a separate time period of clock separation. See In re Wands, *858 F.2d 731, 737, 8 USPQ2d 1400, 1404 (Fed. Cir. 1998) as appropriate. See also MPEP § 2164.01(a) and § 2164.04.*

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 35 is rejected under 35 U.S.C. 102 (b) as being anticipated by Balakrishnan et al (USP 5,101,347).

Regarding claim 35, Balakrishnan discloses a data transmitter (and a receiver) configured and arranged to receive a plurality of input signals and to transmit a plurality of first output signals and a plurality of second output signals (abstract; parallel transmission of digital data) (col. 3, lines 4-6), each of the first and second output signals (a plurality of output signals) corresponding to a different one of the input signals and each being transmitted along a corresponding one of a plurality of conductive paths (each transmitter or transmission path is separate from the other, see fig. 2; col. 3, lines 29-35), said data transmitter comprising:

a signal transmitter for sending each one of the plurality of first and second output signals on a respective one of substantially parallel conductors of a bus (fig. 2; col. 3, lines 29-48), with transmissions on each one of the substantially parallel conductor separated by a time period substantially equal to a clock period T_CLK (transmission path is compensated for by providing a controlled delay path (delay generator, a delay created as a result of the path delay, see abstract; the path delay is designed so as to generate a path that is longer than any data path delay in the device, col. 2, lines 23-26); and

a delay generator for delaying said second output signals by a delay period T_DLY relative to said first output signals so that a first time between a transition on an input signal and a corresponding transition on a corresponding second output signal exceeds a second time between a transition on an input signal and a corresponding transition on a corresponding first output signal by the delay period T_DLY (delay generator whereby a delay is created as a result of the path delay, see abstract; the path delay is designed

so as to generate a path delay that is longer than any data path delay in the device, col. 2, lines 23-26), wherein the clock period T_CLK is greater than the delay period T DLY (a delay of x-secs (24 nsec in this case delay generated or built in) to ensure via control strobe to limit data rate to about 40 million transfers per second) (col. 1, lines 60-68; col. 2, lines 9-39), and wherein adjacent conductive paths that each carry one of the plurality of first output signals are separated by a conductive path that carries one of the plurality of second output signals (delay generated designed to provide 24 nsec of delay to ensure via control strobe to limit data rate to about 40 million transfers per second) (col. 1, lines 60-68; col. 2, lines 9-39).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 12-20, are rejected under 35 U.S.C. 103 (a) as being unpatentable over Balakrishnan et al (USP 5,101,347) in view of Hamamoto et al (IEEE paper, May 1998).

Regarding claim 12, Balakrishnan discloses substantially all limitations of the claim above, except does not explicitly disclose a plurality of first latches, each having (1) a clock input configured and arranged to receive a first clock signal including a series of first transitions, with consecutive first transitions being separated by a time period T_CLK, (2) a latch input configured and arranged to receive a corresponding one

of the input signals, and (3) an latch output configured and arranged to produce a corresponding latch signal, each first latch being further configured and arranged to latch a data value from the corresponding input signal to the corresponding latch signal upon each first transition; and

a plurality of second latches, each having (1) a clock input configured and arranged to receive a second clock signal based on the first clock signal and including a series of second transitions, with consecutive second transitions being separated by a time period T_CLK, (2) a latch input configured and arranged to receive a corresponding input signal, and (3) a latch output configured and arranged to produce a corresponding latch signal, each second latch being further configured and arranged to latch a data value from the corresponding input signal to the corresponding latch signal upon each second transition. However, Hamamoto et al discloses a plurality of first latches (fig. 4, F and B latches), each having (1) a clock input configured and arranged to receive a first clock signal including a series of first transitions (tin (rise and fall), with consecutive first transitions being separated by a time period T_CLK (f-CLK and B-CLK, separated via variable delay line), (2) a latch input configured and arranged to receive a corresponding one of the input signals, and (3) an latch output configured and arranged to produce a corresponding latch signal, each first latch being further configured and arranged to latch a data value from the corresponding input signal to the corresponding latch signal upon each first transition (page 771, section B; page 772, first column and second column); and a plurality of second latches, each having (1) a clock input configured and arranged to receive a second clock signal based on the first clock signal

and including a series of second transitions, with consecutive second transitions being separated by a time period T_CLK, (2) a latch input configured and arranged to receive a corresponding input signal, and (3) a latch output configured and arranged to produce a corresponding latch signal, each second latch being further configured and arranged to latch a data value from the corresponding input signal to the corresponding latch signal upon each second transition (fig. 4; page 771, section B; page 772, first column and second column), wherein each first output signal is based on a latch signal of a different one of the first latches and each second output signal is based on a latch of a different one of the second latches (see fig. 4, F-Latch and B-Latch with inputs and outputs). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teachings of Hamamoto in the system of Balakrishnan because it simplify the estimation of valid transition and aligns clock to center point of valid data as a result input data skew can be compensated resulting in transfer of data at a higher speed.

Regarding claims 13, Balakrishnan discloses data transmitter and the plurality of conductive paths are fabricated on the same semiconductor substrate (col. 4, lines 13-18).

Regarding claim 14, the limitation data transmitter is further configured and arranged to receive an operating voltage from two power rails, and wherein the two power rails are parallel to and on opposite sides of the plurality of conductive paths is well known, power and ground return lines are separation is a common occurrence in design practice to provide communication and transfer of signals with minimum

crosstalk and noise coupling by separating the power lines or planes such as top and bottom of circuit boards and therefore an obvious choice to a person of ordinary skill in the art to utilize the common knowledge available in the design circle.

Regarding claim 15, Balakrishnan discloses each one among the plurality of conductive paths includes a corresponding one of a plurality of parallel transmission lines, and wherein the data transmitter is further configured and arranged to couple the first clock signal to one of the plurality of parallel transmission lines (col. 3, lines 13-55).

Regarding claim 16 Balakrishnan discloses substantially all limitations of the claim above, except does not disclose a plurality of buffer coupled to a different one of the latch outputs of the first and second latches. However, Hamamoto, discloses a number of buffers arranged to provide bufferto each of the plurality of latches (fig. 4). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the teachings of Hamamoto to provide buffers to each of the plurality of latches in the system of Balakrishnan because it can simplify the estimation of valid transition and aligns clock to center point of valid data as a result input data skew can be compensated resulting in transfer of data at a higher speed.

Regarding claim 17, Balakrishnan discloses data transmitter further comprising a delay element configured and arranged to receive the first clock signal and to produce the second clock signal, wherein the second clock signal is delayed with respect to the first clock signal by the delay period T_DLY (col. 2, lies 10-39, fig. 2).

Regarding claim 19, Balakrishnan discloses wherein the second clock signal is substantially identical to the first clock signal (fig. 3).

Regarding claim 20, Balakrishnan discloses the delay period T_DLY is at least as long as a rise time of the data clock signal (col. 2, lines 10-39).

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutbuddin Ghulamali whose telephone number is (571)-272-3014. The examiner can normally be reached on Monday-Friday, 7:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

QG
November 11, 2010.

/CHIEH M FAN/
Supervisory Patent Examiner, Art Unit 2611